ADVANCE INFORMATION

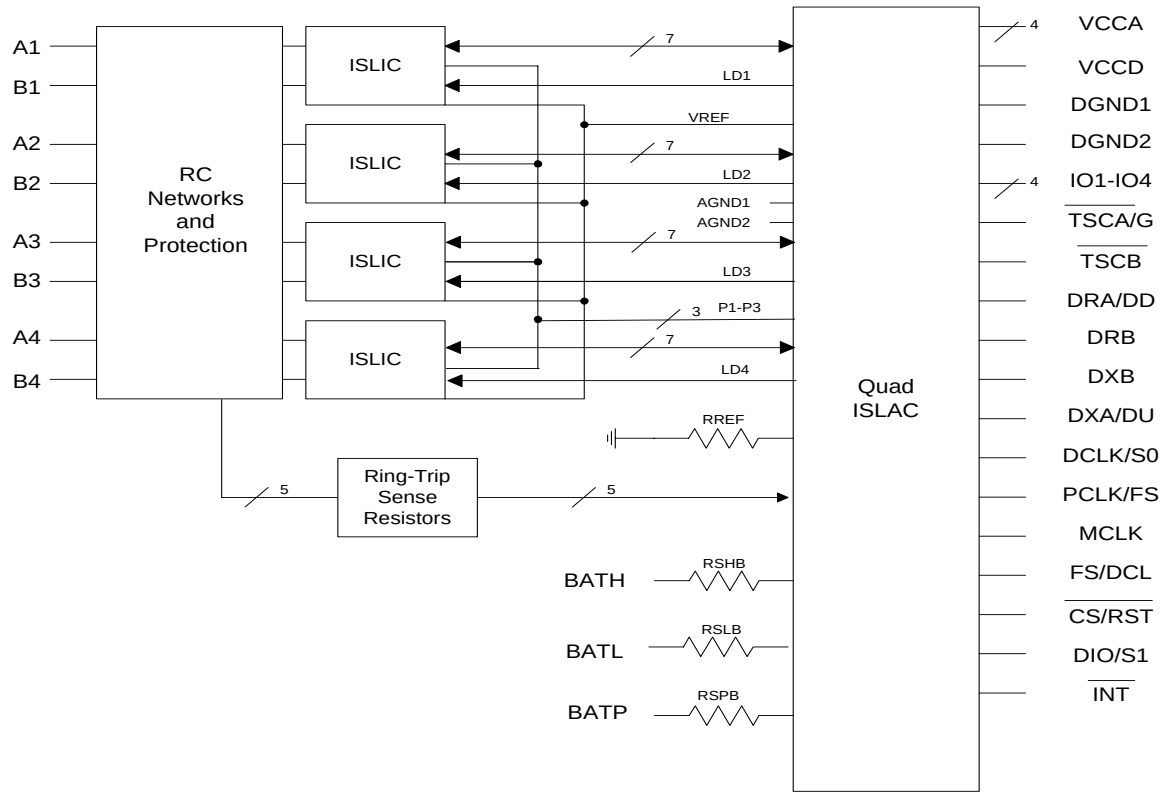
Am79Q2241/2242/2243

Quad Intelligent Subscriber Line Audio-Processing Circuit (ISLAC™)

DISTINCTIVE CHARACTERISTICS

- **High performance digital signal processor provides programmable control of all major linecard functions**
  - — A/μ-law and linear codec
    - — Transmit and receive gain
    - — Two-wire AC impedance
    - — Trans-hybrid balance
    - — Equalization
  - — DC loop feeding
    - — Smooth or abrupt polarity reversal
  - — Loop supervision
    - — Off-hook debounce circuit
    - — Ground-key and ring-trip filters
  - — Ringing generation and control
  - — Adaptive hybrid balance
  - — Line and circuit testing
  - — Tone generation
  - — Metering generation at 12 kHz and 16 kHz
    - — Envelope shaping and level control
- **Selectable PCM/MPI or GCI digital interfaces**
  - — Supports most available master clock frequencies from 512 kHz to 8.196 MHz
- **General purpose I/O pins**
- **0 to 70°C commercial operation**
  - — –40°C to 85°C extended temperature range available
- **+3.3 V DC operation**
- **Exceeds LSSGR and ITU requirements**
- **Supports external ringing with on-chip ring-trip circuit**
  - — Automatic or manual ring-trip modes

BLOCK DIAGRAM



Pub. # **22421** Rev**: A** Amendment**: /0**
Issue Date: **September 1998**

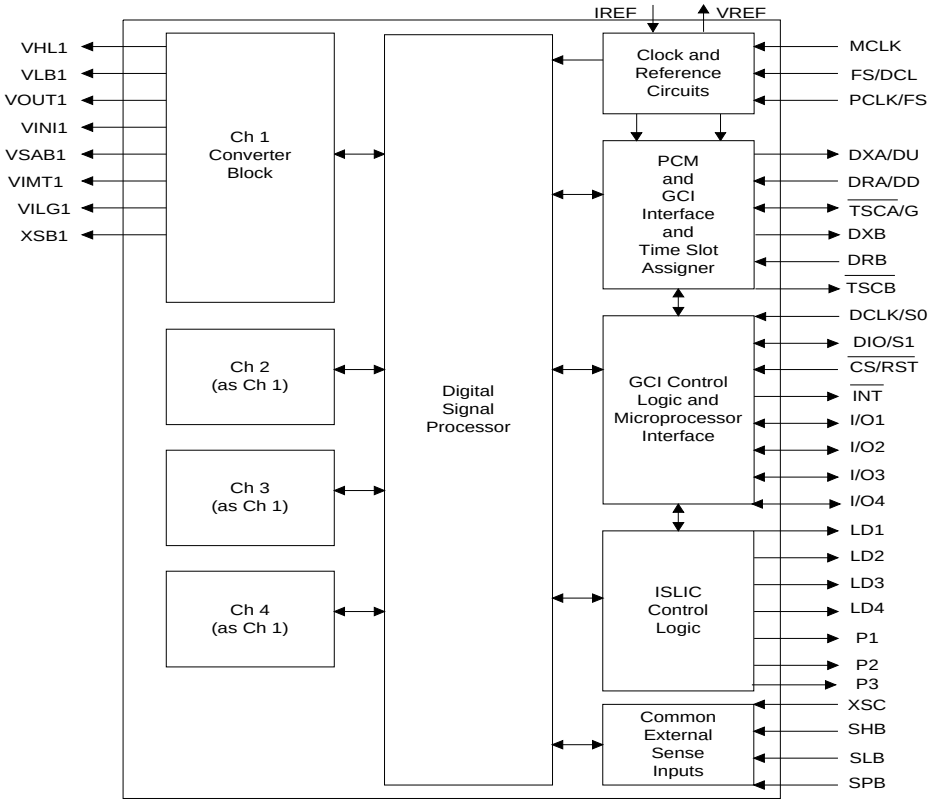
TABLE OF CONTENTS

The quad ISLAC device, in combination with an ISLIC™ device, implements a four channel universal telephone line interface. This enables the design of a single, low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces. Additionally, the quad ISLAC device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective.

DISTINCTIVE CHARACTERISTICS OF THE INTELLIGENT ACCESS VOICE CHIPSET

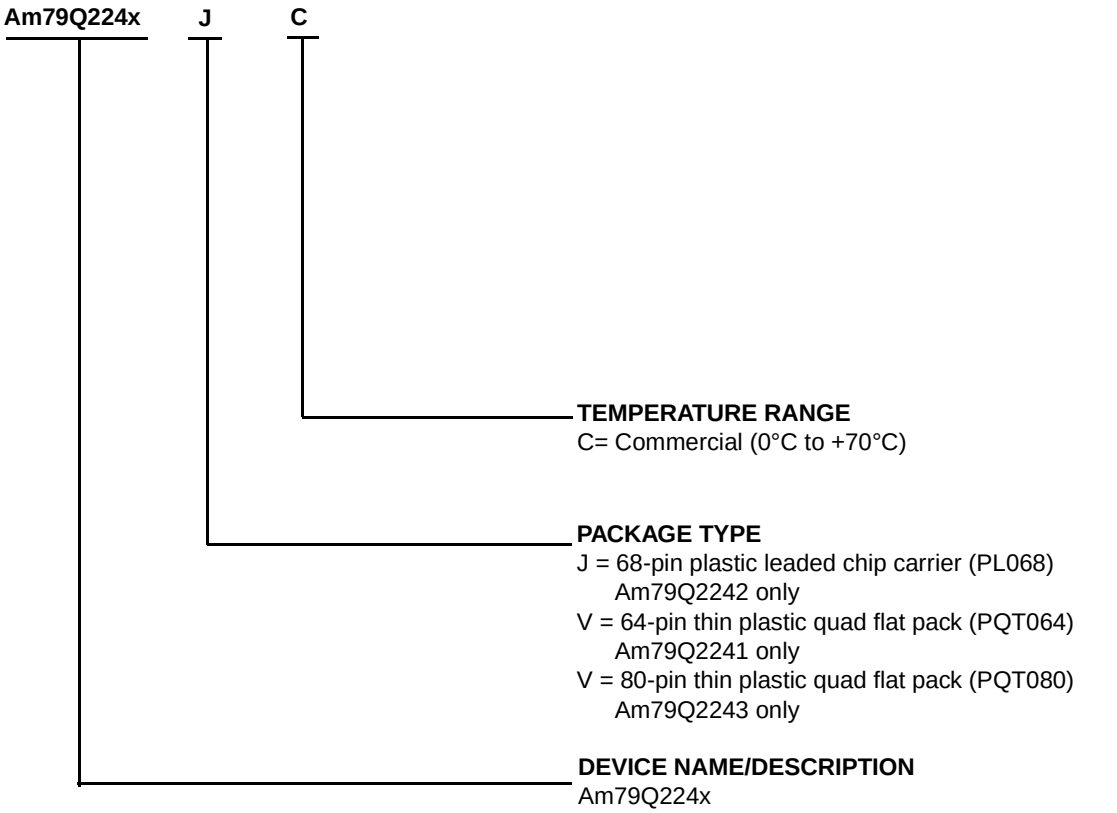
- **Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions**
- **Two chip solution supports high density, multi-channel architecture**
- **Single hardware design meets multiple country requirements through software programming of:**
  - — Ringing waveform and frequency
  - — DC loop-feed characteristics and current-limit
  - — Loop-supervision detection thresholds
    - — Off-hook debounce circuit
    - — Ground-key and ring-trip filters
  - — Off-hook detect de-bounce interval
  - — Two-wire AC impedance
  - — Trans-hybrid balance
  - — Transmit and receive gains
  - — Equalization
  - — Digital I/O pins
  - — A/μ-law and linear selection
- **Supports internal and external ringing**
  - — Self-contained ringing generation and control
  - — Supports external ringing generator and ring relay
  - — Ring relay operation synchronized to zero crossings of ringing voltage and current
  - — Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- **Supports metering generation with envelope shaping**
- **Smooth or abrupt polarity reversal**
- **Adaptive trans-hybrid balance**
  - — Continuous or adapt and freeze
- **Supports both loop-start and ground-start signaling**
- **Exceeds LSSGR and CCITT central office requirements**
- **Selectable PCM or GCI interface**
  - — Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- **On-hook transmission**
- **Power/service denial mode**
- **Line-feed characteristics independent of battery voltage**
- **Only 5 V, 3.3 V and battery supplies needed**
- **Low idle-power per line**
- **Linear power-feed with intelligent power-management feature**
- **Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance**
- **Monitors two-wire interface voltages and currents for subscriber line diagnostics**
- **Built-in voice-path test modes**
- **Power-cross, fault, and foreign voltage detection**
- **Integrated line-test features**
  - — Leakage
  - — Line and ringer capacitance
  - — Loop resistance
- **Integrated self-test features**
  - — Echo gain, distortion, and noise
- **0 to 70°C commercial operation**
  - — –40°C to 85°C extended temperature range available
- **Small physical size**
- **Up to three relay drivers per ISLIC device**
  - — Configurable as test load switches

Figure 1. Quad ISLAC Block Diagram



ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The ordering number (valid combination) is formed by a combination of the elements below. Four ISLIC devices need to be used with this part.



Valid Combinations	
Am79Q2241	VC
Am79Q2242	JC
Am79Q2243	VC

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

CONNECTION DIAGRAMS

Figure 2. 68-Pin PLCC Connection Diagram

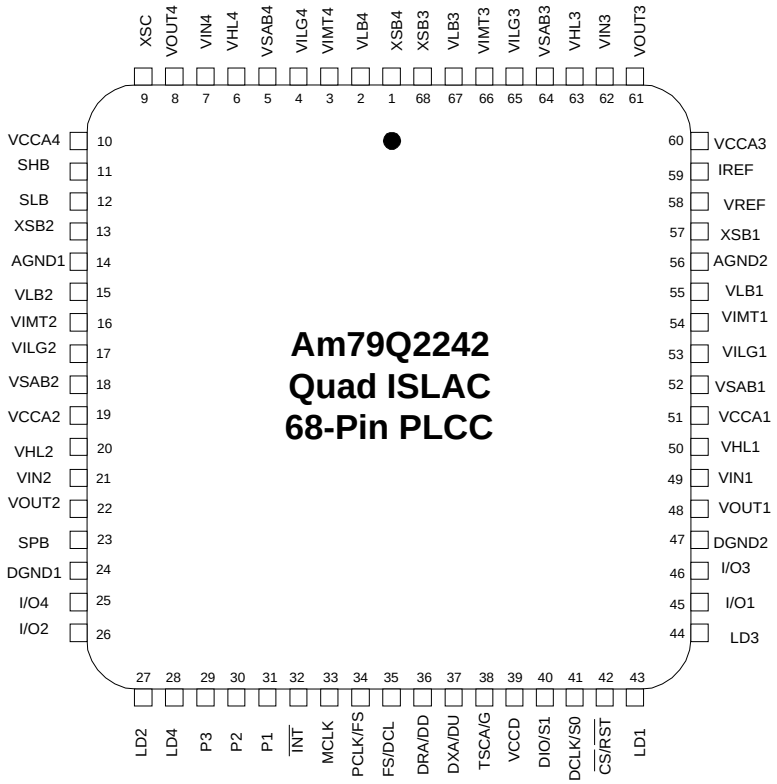


Figure 3. 64-Pin TQFP Connection Diagram

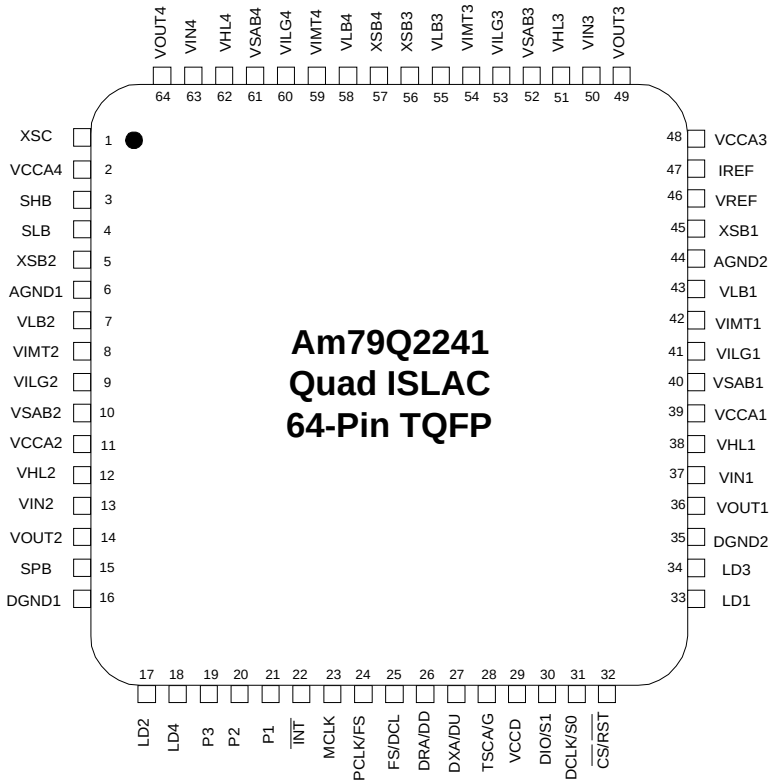
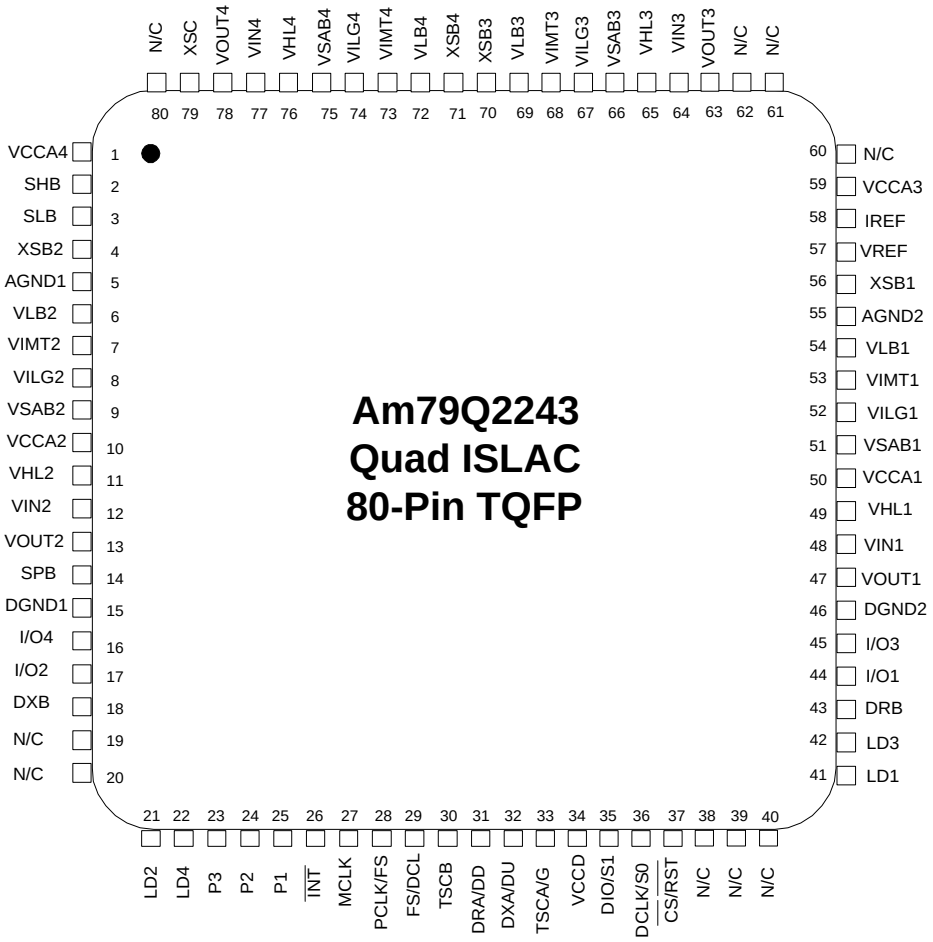


Figure 4. 80-Pin TQFP Connection Diagram



PIN DESCRIPTIONS

Pin	Pin Name	I/O	Description
AGND1, AGND2	Analog Ground	O	Analog circuitry ground returns
DCLK/S0	Data Clock/GCI Address Strap 0	I	Provides data control for MPI interface control. For GCI operation, this pin is device address bit 0. 5 V tolerant.
DGND1–DGND2	Digital Ground		Digital ground returns
DIO/S1	Data I/O/GCI Address Strap 1	I/O	For PCM backplane operation, control data is serially written into and read out of the ISLAC device via the DIO pin with the MSB first. The data clock (DCLK) determines the data rate. DIO is high impedance except when data is being transmitted from the ISLAC device under control of $\overline{CS}$/$\overline{RST}$. For GCI operation, this pin is device address bit 1. 5 V tolerant.
DRA/DD, DRB	RX Path A Backplane Data/ GCI data Downstream, Receive Path B backplane data	I	For the PCM highway, the receive PCM data is input serially through the DRA or DRB ports. The data input is received every 125 µs and is shifted in, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. The receive port can receive information for direct control of the ISLIC device. This mode is selected in Device Configuration Register 2 (RTSEN=1, RTSMD=1). When selected, this data is received in an independently programmable timeslot from the PCM data. For the GCI mode, downstream receive and control data is accepted on this pin. The DRB pin is available only on the 80-pin TQFP package. 5 V tolerant.
DXA/DU, DXB	TX Path A Backplane Data/GCI Data Upstream, TX Path B Backplane Data	O	For the PCM highway, the transmit PCM data is transmitted serially through the DXA or DXB ports. The transmission data output is available every 125 µs and is shifted out, MSB first, in 8-bit PCM or 16-bit linear bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the inactive mode. Can also select a mode (RTSEN= 1, RTSMD=1 or 0 in Device Configuration Register 2) that transmits the Signaling Register MSB contents first, in an independently programmable timeslot from the PCM data. This data is transmitted in all modes except disconnect. For the GCI mode, upstream transmit and signaling data is transferred on this pin. The DXB pin is available only on the 80-pin TQFP package. 5 V tolerant.
FS/DCL	Frame sync/GCI Downstream Clock	I	For PCM operation, pin is Frame Sync. PCM operation is selected by the presence of an 8 kHz Frame Sync signal on this pin in conjunction with the PCLK on the PCLK/FS pin (see below). This 8 kHz pulse identifies the beginning of a frame. The ISLAC device references individual timeslots with respect to this input, which must be synchronized to PCLK. GCI operation is selected by the presence of the downstream clock DCL, on this pin in conjunction with the presence of a FS on the PCLK/FS pin. In GCI mode, the rate at which data is shifted into or out of the PCM ports is a derivative of this DCL clock as selected in Device Configuration Register 1. 5 V tolerant.
$\overline{INT}$	Interrupt	O	For PCM operation, when a subscriber line requires service, this pin goes to a logic 0 to interrupt a higher level processor. Several registers work together to control operation of the interrupt: Signaling and Global Interrupt Registers with their associated Mask Registers, and the Interrupt Register. See the description at configuration register 6 (Mask) for operation. Logic drive is selectable between open drain and TTL-compatible outputs.
I/O1–I/O4	Control Ports	I/O	General purpose, TTL-compatible, logic input/output connection for each of 4 channels. These control lines are TTL-compatible and each can be programmed as an input or output in the Global I/O Direction Register. When programmed as outputs, they can control an external logic device. When programmed as inputs, they can monitor external, TTL-compatible logic circuits. Data for these pins can be written or read individually (from the channel specific I/O Register) or as a group (from the Global I/O Data Register). Not available on the 64-pin package.
IREF	Current Reference	I	External resistor (RREF) connected between this pin and analog ground generates an accurate, on-chip reference current for the A/D's and D/A's on the ISLAC chip.
LD1–LD4	Register Load	O	The LD pins output 3-level voltages. When LDn is a logic 0, the destination of the code on P1–P3 is the relay control latches in the ISLIC control register. When LDn is a logic 1, the destination of P1–P3 is the mode control latches. LDn is driven to VREF when the contents of the ISLIC control register must not change.
MCLK	Master Clock	I	For PCM backplane operation, a DSP master clock connects here. A signal is required only for PCM backplane operation when PCLK is not used as the master clock. MCLK can be a wide variety of frequencies. Upon initialization the MCLK input is disabled, and relevant circuitry is driven by a connection to PCLK. The MCLK connection may be re-established under user control. 5 V tolerant.

Pin	Pin Name	I/O	Description
PCLK/FS	PCM Clock/Frame Sync	I	For PCM operation, this is PCM Clock. PCM operation is selected by the presence of a PCLK signal on this pin in conjunction with the FS on the FS/DCL pin (see below). For PCM backplane operation, connect a data clock, which determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK can be any multiple of the FS frequency. The minimum clock frequency for linear/ companded data plus signaling data is 256 kHz. For GCI operation, this pin is Frame Sync. The FS signal is an 8 kHz pulse that identifies the beginning of a frame. The ISLAC device references individual timeslots with respect to this input, which must be synchronized to DCL. 5 V tolerant.
P1–P3	HVASLIC Control	O	Control the operating modes of the four ISLIC devices connected to the quad ISLAC device.
$\overline{CS}$/$\overline{RST}$	Chip Select/Reset	I	For PCM backplane operation, a logic low on this pin for 15 or more DCLK cycles resets the sequential logic in the ISLAC device into a known mode. A logic low placed on this pin for less than 15 DCLK cycles is a chip select and enables serial data transmission into or out of the DIO port. For GCI operation, a logic low on this pin—for 1 ms or longer—resets the sequential logic into a known mode. See Table 2-4 in the Technical Reference for details. 5 V tolerant.
SHB, SLB, SPB	Battery Sense	I	Resistors that sense the high, low and positive battery voltages connect here. If only one negative battery is used, connect both resistors at the supply. If the positive battery is not used, leave the pin unconnected. These pins are current inputs whose voltage is held at VREF.
$\overline{TSCA}$/G, $\overline{TSCB}$	Timeslot Control A/GCI Mode, Time Slot Control B	O (PCM) I (GCI)	For PCM backplane operation, $\overline{TSCA}$ or $\overline{TSCB}$ is active low when PCM data is output on the DXA or DXB pins. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VCCD. $\overline{TSCB}$ is only available on the 80 pin TQFP package. When GCI mode is selected, one of two GCI modes may be selected by connecting $\overline{TSCA}$/G to DGND or VCCD.
VSAB1–VSAB4	Loop voltage sense	I	Connect to the VSAB pins of four ISLIC devices.
VCCA1–VCCA4	Power Supply		+3.3 VDC supplies to the analog sections in each of the four channels.
VCCD	Power Supply		+3.3 VDC supply to all digital sections.
VREF	Analog Reference	O	This pin provides a 1.4 V, single-ended reference to the four ISLIC devices to which the ISLAC device is connected.
VHL1–VHL4	High Level D/A	O	High-level loop control voltages on these pins are used to control DC-feed, internal ringing, metering and polarity reversal for each ISLIC device.
VIN1–VIN4	TX Analog	I	Analog transmit signals (VTX) from each ISLIC device connect to these pins. The ISLAC device converts these signals to digital words and processes them. After processing, they are multiplexed into serial time slots and sent out of the DXA/DU pin.
VLB1–VLB4	Longitudinal Reference	O	Normally connected to VCCA internally. They supply longitudinal reference voltages to the ISLIC devices during certain test procedures. These outputs are connected internally to VCCA during ISLIC Active, Standby, Ringing, and Disconnect modes. During test modes, it can be connected to the receive D/A.
VIMT1–VIMT4, VILG1–VILG4	Sense	I	The IMT and ILG pins of four ISLIC devices connect to the VIMT1–VIMT4 and VILG1–VILG4 pins of the ISLAC chip. These pins are voltage inputs referenced to VREF. They require external resistors connected between each pin and VREF to convert IMTn and ILGn into voltages.
VOUT1–VOUT4	RX Analog	O	The ISLAC device extracts and processes voice data from time slots on DRA/DD serial data port. After processing, the ISLAC device converts the voice data to analog signals that are sent out of these pins to each respective ISLIC device.
XSB1–XSB4	External Sense	I	External resistors connect here that sense an external voltage. In a linecard with external ringing, they are used to sense the voltage at the line side of the ring-feed resistor.These pins are current inputs whose voltage is held at VREF. An internal resistor converts currents flowing in these pins into voltages to be sampled by the A/D.
XSC	Common External Sense	I	An external resistor connects here that senses a common reference for external voltages sensed by resistors connected to XSB1–XSB4.This pin is a current input whose voltage is held at VREF. An internal resistor converts current flowing in this pin into a voltage to be sampled by the A/D. This pin is intended for sensing external ringer supply voltages. However, it can also be used to sense other test points when internal ringing is used.

Pin Options	Package Type		
	80 pin	68 pin	64 pin
DRB	√	x	x
DXB	√	x	x
$\overline{\text{TSCB}}$	√	x	x
I/O1–I/O4	√	√	x

GENERAL DESCRIPTION

The Intelligent Access voice chipsets integrate all functions of the subscriber line for four subscriber lines. One or more of two chip types are used to implement the linecard; an ISLIC device and a quad ISLAC device. These provide the following basic functions:

1. The ISLIC device: A high voltage, bipolar IC that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The quad ISLAC device: A low voltage CMOS IC that provides conversion and DSP functions for all 4 channels.

Complete schematics of linecards using the Intelligent Access voice chipsets for internal and external ringing are shown in Figure 5 and Figure 6.

The ISLIC device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ISLAC device to operate in eight different modes that control power consumption and signaling modes. This enables it to have full control over the subscriber loop. The ISLIC device is customized to be used exclusively with the ISLAC device as part of a multiple-line chipset. The ISLIC device requires only +5 V power and the battery supplies for its operation.

The ISLIC device implements a linear loop-current feeding method with the enhancement of intelligent thermal management in a controlled manner. This limits the amount of power dissipated on the ISLIC chip by dissipating excess power in external resistors.

Each ISLAC device contains high-performance codec circuits that provide A/D and D/A conversion for voice (codec), DC-feed and supervision signals for four subscriber channels. The ISLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all four channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The Intelligent Access voice chipsets provide a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics. In addition, it provides system level solutions for the loop supervisory functions and metering. In total, the chipset provides a programmable solution that can satisfy worldwide linecard requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with the WinSLAC™ software. This PC software is provided free of charge. It allows the designer to enter a description of system requirements. WinSLAC then returns the necessary data and plots the predicted system results.

The ISLIC interface unit inside the ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the ISLAC device to place several key ISLIC performance parameters under software control.

The main functions that can be observed and/or controlled through the ISLAC backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth battery reversal
- Subscriber line matching
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the ISLIC device collects the following information and feeds it, in analog form, to the ISLAC device:

- The metallic and longitudinal loop currents
- The AC and DC loop voltage

The outputs supplied by the ISLAC device to the ISLIC device are then:

- A voltage that provides control for the following high-level ISLIC device outputs:
  —DC loop current
  —Internal ringing signal
  —12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal
- A voltage that controls longitudinal offset for test purposes

The ISLAC device performs the codec and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the trans-hybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive trans-hybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

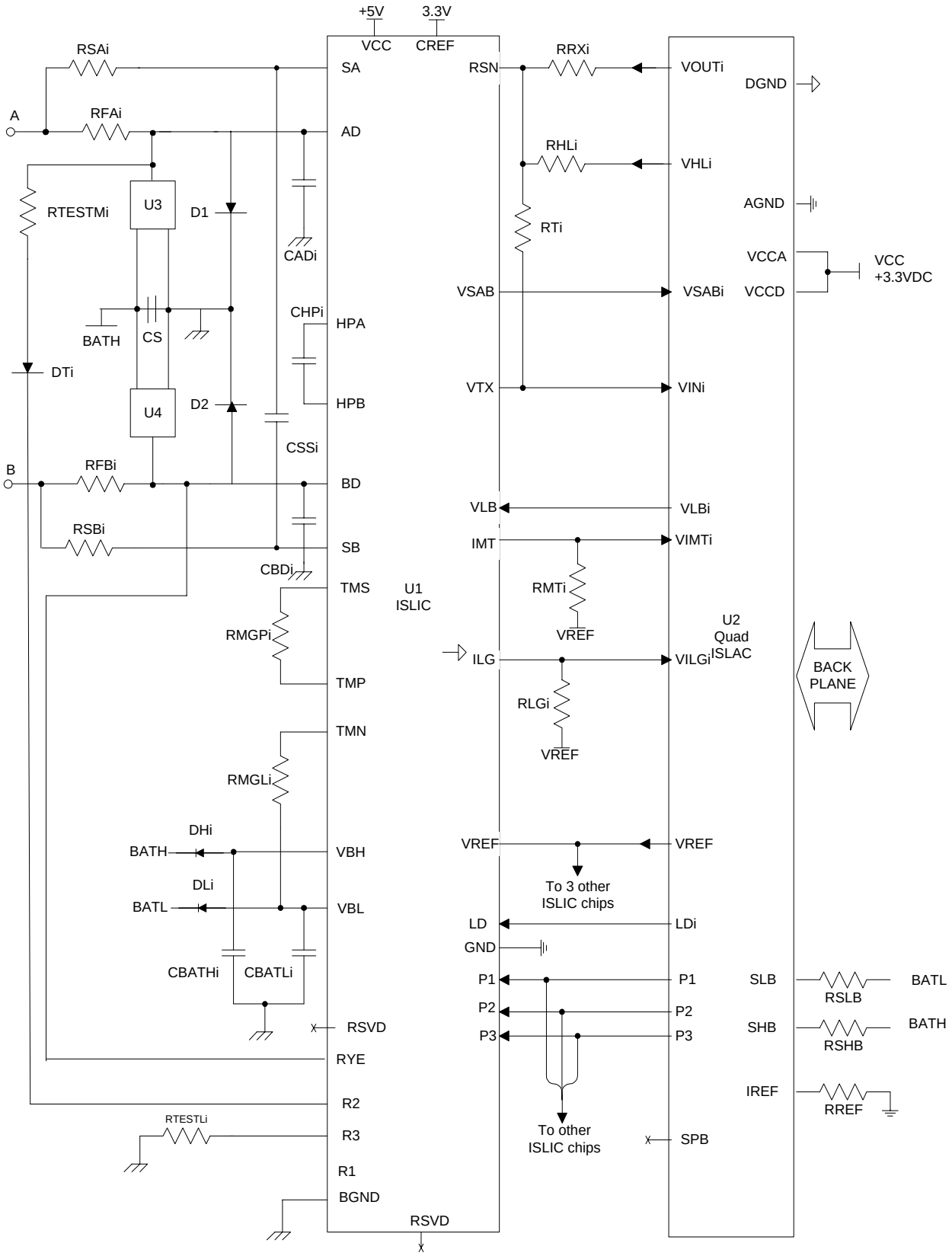
Besides the codec functions, the Intelligent Access voice chipset provides all the sensing, feedback, and clocking necessary to completely control ISLIC device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The ISLAC device supplies complete mode control to the ISLIC device using the control bus and tri-level load signal.

The Intelligent Access voice chipset provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

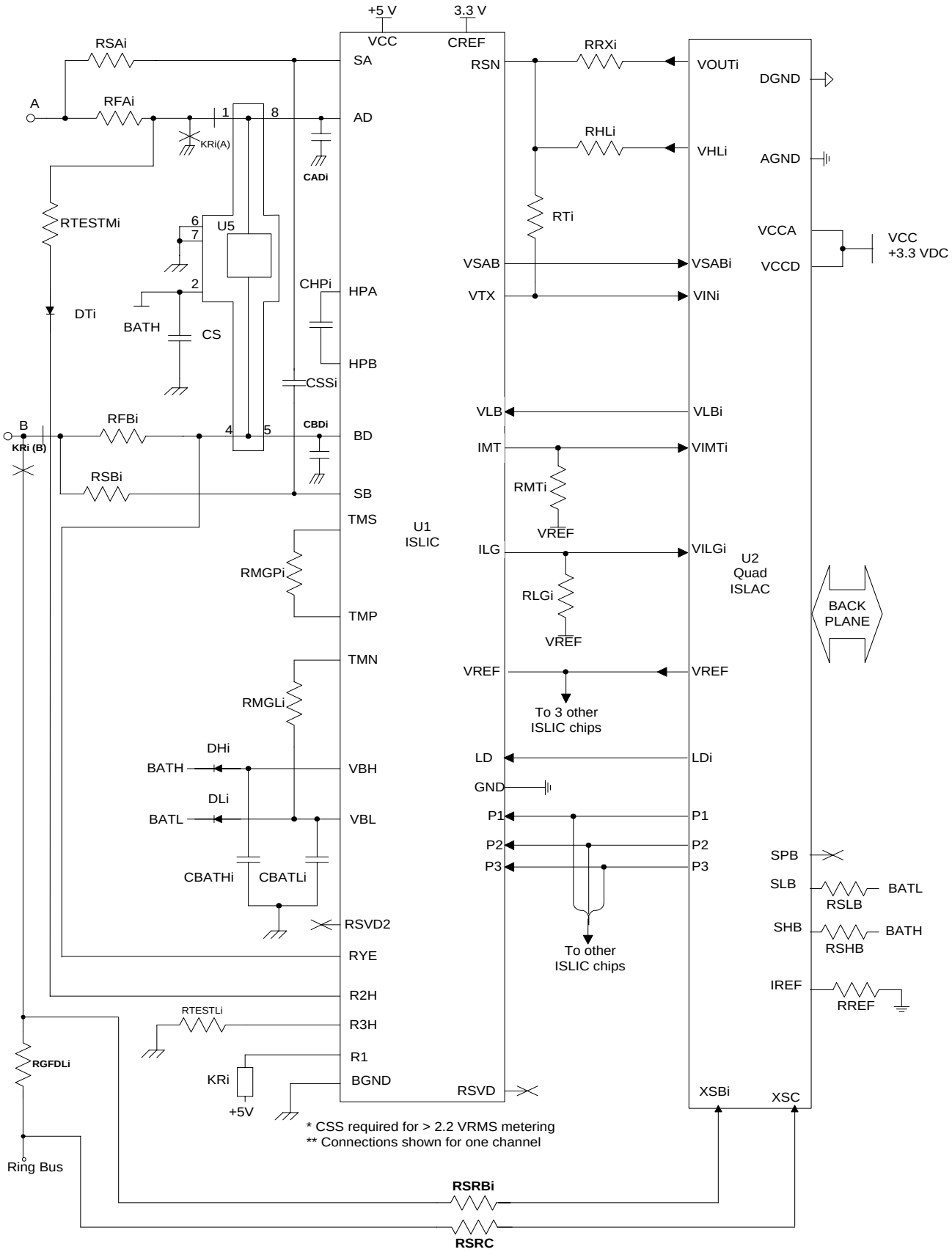
For subscriber line diagnostics, AC and DC line conditions can be monitored using built in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual PCM measurement data directly to a higher level processor by way of the voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

Figure 5. Internal Ringing Linecard Schematic



* CSS required for > 2.2 VRMS metering
** Connections shown for one channel

Figure 6. External Ringing Linecard Schematic



LINECARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the linecard (i = 1,2,3,4)

Item	Type	Value	Tol.	Rating	Comments
U1	Am79R241				ISLIC device
U2	Am79X22xx				ISLAC device
U3, U4	P1001SC			100 V	TECCOR Battrax protector
U5	TISP61089			80 V	Transient Voltage Suppresser, Power Innovations
D1, D2	Diode	1 A		100 V	
DHi, DLi, DTi	Diode	100 mA		100 V	50 ns
RFAi, RFBi	Resistor	50 Ω	2%	2 W	Fusible PTC protection resistors
RSAi, RSBi	Resistor	200 kΩ	2%	1/4 W	Sense resistors
RTi	Resistor	80.6 kΩ	1%	1/8 W	
RRXi	Resistor	100 kΩ	1%	1/8 W	
RREF	Resistor	69.8 kΩ	1%	1/8 W	Current reference
RMGLi, RMGPi	Resistor	1 kΩ	5%	1 W	Thermal management resistors
RSHB, RSLB	Resistor	750 kΩ	0.5%	1/8 W	
RHLi	Resistor	5.1 kΩ	0.5%	1/8 W	
RMTi	Resistor	3.01 kΩ	0.5%	1/8 W	
RLGi	Resistor	6.04 kΩ	0.5%	1/8 W	
RTESTMi	Resistor	2 kΩ	1%	1 W	Metallic test
RTESTLi	Resistor	2 kΩ	1%	1 W	Longitudinal test
CADi, CBDi [1]	Capacitor	22 nF	10%	100 V	Ceramic, not voltage sensitive
CBATHi, CBATLi	Capacitor	100 nF	20%	100 V	Ceramic
CHPi	Capacitor	22 nF	20%	100 V	Ceramic
CSi[1]	Capacitor	100 nF	20%	100 V	Protector speed up capacitor
CSSi[3]	Capacitor	56 pF	5%	100 V	Ceramic
Components for External Ringing					
RGFDi	Resistor	510 Ω	2%	2 W	1.2 W typ
RSRBi, RSRc	Resistor	750 kΩ	2%	1/4 W	Matched to within 0.2% for initial tolerance and 0 to 70° C ambient temperature range.[2] 17 mW typ
KRi	Relay	5 V Coil			DPDT

Note: *1. Value can be adjusted to suit application.*

2. Can be looser for relaxed ring-trip requirements. 1% match (each resistor ±1%) gives 1.275 mA uncertainty in ringing current sensing.

3. Required for metering > 2.5 Vrms, otherwise may be omitted.